We claim:

1. A method for selective etching in the manufacture of a semiconductor device, comprising the steps of:

- forming a layer of amorphous silicon-germanium on a substrate of monocrystalline silicon or on a substrate at least comprising a surface layer of monocrystalline silicon,

- depositing at least one dielectric layer on the amorphous silicon-germanium layer so as to prevent crystallization of the amorphous layer;

- patterning the resultant structure, and etching the dielectric layer and the amorphous silicon-germanium layer within a predetermined region; and

- heat-treating the resultant structure subsequent to etching so as to crystallize the amorphous layer.

2. The method as claimed in claim 1, wherein the amorphous silicon-germanium layer is formed by simultaneous deposition of silicon and germanium.

3. The method as claimed in claim 1, wherein the amorphous silicon-germanium layer is formed by deposition of silicon followed by implantation of germanium.

4. The method as claimed in claim 1, wherein the amorphous silicon-germanium layer is formed with a germanium content of between 5 and 60 atomic percent, more preferably between 10 and 55 atomic percent and most preferably between 30 and 50 atomic percent.

5. The method as claimed in claim 1, wherein the silicon germanium layer is formed as a multilayer structure, wherein each layer has an individual material composition.

6. The method as claimed in claim 1, wherein the amorphous silicon-germanium layer is doped.

7. The method as claimed in claim 6, wherein the amorphous silicon-germanium layer is doped by ion implantation, preferably with B^{11} or BF_2.

8. The method as claimed in claim 7, wherein the amorphous silicon-germanium layer is doped simultaneously as it is formed on the substrate.

9. The method as claimed in claim 1, wherein the amorphous silicon-germanium layer is formed on the substrate by using any one of the techniques CVD, RP-CVD, UHV-CVD and MBE.

10. The method as claimed in claim 1, wherein the dielectric layer is deposited by any one of the techniques PE-CVD, SA-CVD, HDP-CVD, MBE or a spin-on technique.

11. The method as claimed in claim 1, wherein the dielectric layer is a TEOS.

12. The method as claimed in claim 1, wherein the dielectric layer is deposited at a temperature of between 250 and 400°C.

13. The method as claimed in claim 1, wherein the amorphous silicon-germanium layer is etched within a predetermined region using a fluorine-or chlorine-based chemistry.

14. The method as claimed in claim 1, wherein the amorphous silicon-germanium layer is patterned and etched in order to produce a polyresistor having very low temperature dependence.

15. The method as claimed in claim 1, wherein said substrate of monocrystalline silicon is p-type doped, particularly with boron, and/or contains germanium.

16. The method as claimed in claim 1, wherein said etching of the amorphous silicon-germanium layer within the predetermined region is a dry etching process and wherein end-point detection of germanium is performed during the dry etching process to control the etching of the amorphous silicon-germanium layer.

17. The method as claimed in claim 16, wherein said end-point detection of germanium is performed by means of emission spectroscopy.

18. The method as claimed in claim 16, wherein said dry etching of the amorphous silicon-germanium layer within the predetermined region is ceased when end-point is detected.

19. The method as claimed in claim 17, wherein said etching of the amorphous silicon-germanium layer within the predetermined region is performed during a short time period, particularly a few seconds, after the end point has been detected in order to safeguard that said layer of amorphous silicon-germanium is etched away completely.

20. The method as claimed in claim 18, further comprising the step of wet etching the amorphous silicon-germanium layer within the predetermined region subsequent to completion of the dry etching process in order to safeguard that said layer of amorphous silicon-germanium is etched away completely.

21. The method as claimed in claim 16, wherein applied etching conditions, particularly parameters such as pressure, gas composition, and bias, during said dry

etching of the amorphous silicon-germanium layer within the predetermined region are altered when end-point is detected.

22. The method as claimed in claim 16, wherein said layer of amorphous silicon-germanium is formed as a multilayer structure, wherein one of the layers closest to the substrate contains germanium, and wherein said performed endpoint detection of germanium is used to detect that said dry etching process has reached to a level in the multilayer structure corresponding to said layer containing germanium.

23. A method in the manufacture of a bipolar transistor having a self-registered base emitter structure, comprising the steps of:

- forming a layer of amorphous silicon-germanium on a substrate of monocrystalline silicon or on a substrate at least comprising a surface layer of monocrystalline silicon,

- depositing at least one dielectric layer on the amorphous silicon-germanium layer so as to prevent crystallization of the amorphous layer;

- patterning the resultant structure, and etching the dielectric layer and the amorphous silicon-germanium layer within a predetermined region; and

- heat-treating the resultant structure subsequent to etching so as to crystallize the amorphous layer,

wherein the substrate includes a buried collector and an epitaxially formed base thereon surrounded by isolation regions, where said predetermined area, within which the dielectric layer and the amorphous silicon-germanium layer are etched, defines an emitter opening above said epitaxially formed base for the bipolar transistor.

24. The method as claimed in claim 23, wherein said epitaxially formed base for the bipolar transistor is p-type doped, particularly with boron, and contains germanium.

25. The method as claimed in claim 23, wherein an oxide is grown or deposited on the structure obtained subsequent to etching.

26. A method in the manufacture of a bipolar transistor having a self-registered base emitter structure, comprising the steps of:

- forming a layer of amorphous silicon-germanium on a substrate of monocrystalline silicon or on a substrate at least comprising a surface layer of monocrystalline silicon,

- depositing at least one dielectric layer on the amorphous silicon-germanium layer so as to prevent crystallization of the amorphous layer;

- patterning the resultant structure, and etching the dielectric layer and the amorphous silicon-germanium layer within a predetermined region; and

- heat-treating the resultant structure subsequent to etching so as to crystallize the amorphous layer,

wherein the substrate includes a buried collector and isolation regions for isolation of said bipolar transistor and where said predetermined region, within which the dielectric layer and the amorphous silicon-germanium layer are etched, defines an emitter opening for said bipolar transistor.

27. The method as claimed in claim 26, wherein an oxide is grown or deposited on the structure obtained subsequently to etching, and a base is formed by means of doping through the oxide.

28. The method as claimed in claim 26, wherein a layer of an electrically insulating material is deposited on the structure obtained subsequent to etching, whereafter the structure is etched an isotropically until a thin oxide layer remains on the substrate in the emitter opening and in such a manner that a spacer of said electrically insulating material remains along the sidewalls of the emitter opening.

29. The method as claimed in claim 28, wherein the electrically insulating material for forming the spacer is comprised of a nitride, which is deposited in a layer of a thickness of a couple of hundred nanometers by LP-CVD technique.

30. The method as claimed in claim 28, wherein an emitter contact is formed in the emitter opening and doped, whereafter the structure is heat-treated to form an emitter base junction in the substrate by means of diffusion of dopants from the emitter contact.

31. The method as claimed in claim 30, wherein the emitter contact is formed by depositing and doping a layer of polycrystalline silicon, whereafter the doped layer is patterned lithographically and plasma etched.

32. A method in the manufacture of an integrated circuit comprising at least a bipolar transistor and a resistor, comprising the steps of:

- forming a layer of amorphous silicon-germanium on a substrate of monocrystalline silicon or on a substrate at least comprising a surface layer of monocrystalline silicon,

- depositing at least one dielectric layer on the amorphous silicon-germanium layer so as to prevent crystallization of the amorphous layer;

- patterning the resultant structure, and etching the dielectric layer and the amorphous silicon-germanium layer within a predetermined region; and

- heat-treating the resultant structure subsequent to etching so as to crystallize the amorphous layer,

wherein the substrate includes a buried collector and isolation regions for isolation of said bipolar transistor and where said predetermined region, within which the dielectric layer and the amorphous silicon-germanium layer are etched, defines an emitter opening for said bipolar transistor, and further comprising the step of:

- depositing a silicon-germanium layer also on the isolation regions, whereby the patterning and etching steps comprise to simultaneously pattern and etch the silicon-germanium layer on top of the isolation regions in order to produce said resistor in the silicon-germanium layer.